162. A method according to claim 34 wherein said semiconductor device is a car navigation system.

163. A method according to claim 34 wherein said semiconductor device is a personal computer.

164. A method according to claim 34 wherein said semiconductor device is a portable information terminal.

165. A method according to claim 35 wherein said semiconductor device is a video camera.

166. A method according to claim 35 wherein said semiconductor device is a digital camera.

167. A method according to claim 35 wherein said semiconductor device is a projector.

168. A method according to claim 35 wherein said semiconductor device is a head mount display.

169. A method according to claim 35 wherein said semiconductor device is a car navigation system.

170. A method according to claim 35 wherein said semiconductor device is a personal computer.

171. A method according to claim 35 wherein said semiconductor device is a portable information terminal.--

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Examiner's Office Action dated July 18, 2001, has been received and its contents reviewed. By this Amendment, claims 15, 17, 20, 22, 25, 28, 30, 31, 34, and 35 have been amended, and new claims 88-171 have been added. Accordingly, claims 15-26, 28 and 30-87 are pending in the present application, of which claims 15, 17, 20, 22, 25 and 28 are independent.

Referring now to the Office Action, claims 15-26, 28, and 30-87 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 5-35 of the copending Application Serial No. 09/352,194, and claims 15-26, 28, and 30-87 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as unpatentable over claims 5-31, 45-68, and 81 of copending Application Serial No. 09/352,373. Applicants respectfully request that these provisional rejections be held in abeyance until all pending claims are in condition for allowance.

Claims 15-24, 28, and 30-87 are rejected under 35 U.S.C. §102(e) as anticipated by Yamazaki et al. (U.S. Patent No. 6,077,731), and claims 25 and 26 are rejected under 35 U.S.C. §103(a) as unpatentable over Yamazaki et al. Applicants respectfully traverse these rejections at least for the reasons provided below.

With respect to the §102(e) rejection of claim 15, the Office Action asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (col. 63, lines 6-8); carrying out a first heat treatment (col. 63, lines 9-20); and, carrying out a second treatment at 900-1100°C in reducing atmosphere (col. 13, lines 41-44, and col. 63, lines 56-61).

Applicants respectfully submit that the Office has misinterpreted Yamazaki et al. Contrary to the Office's assertion that Yamazaki et al. disclose carrying out a second treatment at 900-1100°C in a reducing atmosphere, col. 63, lines 56-61 of Yamazaki et al. states that:

> *"Another heat treatment is implemented in a step in Fig. 30B to form a formal oxide film for gettering the nickel element. This heat treatment is implemented within an atmosphere containing halogen elements. In concrete, this heat treating is implemented within the oxygen atmosphere containing five volume % of HCl. This step is carried out to eliminate the nickel element (or other metal element which promotes crystallization of silicon) which has been introduced intentionally for the crystallization of the initial stage from the crystal silicon film 171...This heat treatment is implemented in a temperature range from 600°C to 750°C.*

Col. 13, lines 41-44 of Yamazaki et al. cited by the Office actually states that the thermal oxide film may be formed in the same temperature range with that of the solid phase crystallization described above, i.e., in the range of about 400-1100°C or preferably about 700-1050°C. Yamazaki et al. further state that the thermal oxide film may be formed in an oxidizing atmosphere, preferably an oxygen atmosphere, an atmosphere containing oxygen, an atmosphere containing a compound which releases oxygen at a temperature in forming the thermal oxide film, or an atmosphere containing oxygen and halogen.

As can be seen, the Office has taken the disclosure of Yamazaki et al. out of context by reciting col. 13, lines 41-44 and col. 63, lines 56-61 as support in a piecemeal manner but still with no disclosure for the step of carrying out a second treatment at 900-1100°C in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film as recited in claim 15.

With respect to the §102(e) rejection of claims 17 and 28, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of adding a catalytic element to at least a portion of the amorphous semiconductor film (col. 63, lines 6-8); carrying out a first heat treatment (col. 63, lines 9-20); and, carrying out a second heat treatment at 900-1100°C in a reducing atmosphere including a halogen element (col. 13, lines 34-44, and col. 63, lines 56-61). However, as discussed above with respect to claim 15, col. 63, lines 56-61 of Yamazaki et al. actually discloses a "second" heat treatment to form a thermal oxide film for gettering the nickel element, wherein the "second" heat treatment is implemented within an atmosphere containing halogen elements in a temperature range from 600°C to 750°C. Again, the Office recited col. 13, lines 41-44 a thermal oxide film formed in an oxidizing atmosphere in the same temperature range with that of the solid phase crystallization in the range of about 400-1100°C, or preferably about 700-1050°C, and in col. 63, lines 56-61, another heat treatment to form a thermal oxide film for gettering the nickel element, wherein the heat treatment is implemented within the oxygen atmosphere containing 5 volume % of HCl.

Applicants respectfully submit that independent claims 17 and 28 distinguish over Yamazaki et al. in reciting the step of carrying out a second heat treatment for the crystalline semiconductor thin film in a reducing atmosphere including a halogen element to flatten a surface of the crystalline semiconductor thin film, as Yamazaki et al. do not disclose this claimed feature..

With respect to the §102(e) rejection of independent claim 20, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of adding a catalytic element to at least a portion of the amorphous silicon semiconductor film (col. 63, lines 6-8); carrying out a first heat treatment (col. 63, lines 9-20); carrying out a second treatment with ultra or infrared light (col. 63, lines 47-50); and carrying out a third treatment at 900-1100°C in a reducing atmosphere including a halogen element (col. 13, lines 34-44, and col. 63, lines 56-61). However, Applicants respectfully submit that, as discussed above, col. 63, lines 56-61 of Yamazaki et al. disclose a "first" and "second" heat treatment, wherein the "second" heat treatment is implemented to form a thermal oxide film for gettering the nickel element in an

oxidizing atmosphere containing 5 volume % of HCl. There is no "third" treatment at 900-1100°C as alleged by the Office. Based on the above-discussed rejections, it would appear that the Office is of the opinion that the "second" treatment is also the "third" treatment in Yamazaki et al.

Moreover, Applicants respectfully submit that claim 20 further distinguishes over Yamazaki et al. in reciting that a second heat treatment is carried out in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film.

With respect to the §102(e) rejection of independent claim 22, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (col. 63, lines 6-8); carrying out a first heat treatment (col. 63, lines 9-20); carrying out a second treatment with ultraviolet or infrared light (col. 63, lines 47-50); and, carrying out a third treatment at 900-1100°C in a reducing atmosphere including a halogen element (col. 13, lines 34-44, and col. 63, lines 56-61).

Again, Applicants respectfully submit that Yamazaki et al. do not disclose a "third" treatment, and that Yamazaki forms a thermal oxide film in an oxidizing atmosphere in the treatment described in col. 13, lines 34-44, and col. 63, lines 56-61, as discussed above. Furthermore, Yamazaki et al. do not disclose carrying out a second treatment with ultraviolet or infrared light. Col. 63, lines 47-50 of Yamazaki et al. disclose that an excimer laser is used.

Applicants further respectfully submit that claim 22 of the present invention further distinguishes over Yamazaki et al. in reciting that a second heat treatment is carried out in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film.

With respect to the §102(e) rejection of claim 32, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of: forming semiconductor film (169)(col. 62, lines 23-25); crystallizing the semiconductor film (col. 63, lines 9-20); etching a surface to remove an oxide (172)(col. 65, lines 15-20); and, heating the semiconductor film in an inactive atmosphere (col. 71, lines 66-67). The Office further asserted that Yamazaki et al. teach that the heating of the semiconductor film in an inactive atmosphere is performed at a temperature of 900-1100°C (col. 13, lines 41-44, and col. 72, lines 10-13).

Applicants respectfully submit that the heat treatment described in col. 71, lines 66-67 of Yamazaki et al. is conducted in order to suppress the influence of carriers moving the sides of the active layers, as described in col. 72, lines 1-3. Applicants respectfully submit the Office has

misinterpreted the disclosure of Yamazaki et al.. Moreover, Applicants respectfully submit that Yamazaki et al. do not disclose the step of heating the semiconductor film after the etching step to form a flattened surface of the semiconductor film.

With respect to the §102(e) rejection of claim 33, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of: forming semiconductor film (169)(col. 62, lines 23-25); crystallizing the semiconductor film (col. 63, lines 9-20); treating a surface of said semiconductor film with hydrofluoric to remove an oxide (172)(col. 65, lines 15-20); and, heating the semiconductor film in an inactive atmosphere (col. 71, lines 66-67). The Office further asserted that Yamazaki et al. teach the heating of the semiconductor film in an inactive atmosphere at the temperature of 900-1100°C (col. 13, lines 41-44, and col. 72, lines 10-13). Applicants respectfully submit that the heat treatment described in col. 71, lines 66-67 of Yamazaki, is conducted in order to suppress the influence of carriers moving the sides of the active layers, as described in col. 72, lines 1-3 of Yamazaki et al. As such, Applicants respectfully submit that the Office has misinterpreted and misapplied Yamazaki et al. in this rejection. Moreover, Yamazaki et al. fail to disclose the step of heating the semiconductor film after the treating step to form a flattened surface of the semiconductor film.

With respect to the §102(e) rejection of claims 30, 31, 34, and 35, these claims have been amended, as shown above, to recite heating the semiconductor film provided with an oxide formed on a surface thereof in an atmosphere which reduces the oxide formed on the surface. Applicants respectfully submit that Yamazaki et al. do not teach, disclose, or suggest using an atmosphere which reduces an oxide formed on a surface on a semiconductor film.

In view of the arguments set forth above, Yamazaki et al. do not positively disclose all the features recited in the rejected claims. Therefore, the § 102(e) rejections of the above discussed claims and their dependent claims are improper and are requested to be reconsidered and withdrawn.

With respect to the §103(a) rejection of claims 25 and 26, the Office asserted that Yamazaki et al. teach a method of forming a TFT device comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (col. 63, lines 6-8); carrying out a first heat treatment (col. 63, lines 9-20); carrying out a second treatment at 900-1100°C in reducing atmosphere (col. 13, lines 41-44, and col. 63, lines 56-61); patterning the crystalline semiconductor (col. 67, lines 52-54); selectively providing the crystalline

semiconductor with phosphorous (col. 69, lines 21-22); and, carrying out a third heat treatment to activate the region into which the impurity ions have been injected (col. 69, lines 27-28).

Applicants respectfully submit that the Office again has misinterpreted and misapplied various teachings of Yamazaki et al., as discussed above, to make the rejection. Moreover, col. 13, lines 41-44, and col. 63, lines 56-61 of Yamazaki discloses forming a thermal oxide film in an oxidizing atmosphere. On the other hand, the presently claimed invention as recited in claim 25 carries out a second heat treatment in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film.

As Yamazaki et al. do not teach, disclose, or suggest carrying out a second heat treatment in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film, the application of Yamazaki in the §103(a) rejection would be improper. Accordingly, the §103(a) rejection of claims 25 and 26 is respectfully requested to be reconsidered and withdrawn.

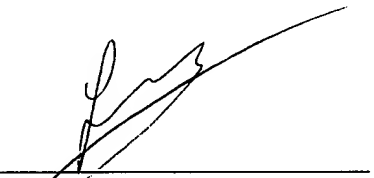
Claims 15-19, 20-24, and 28 are rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claim 1 of Zhang et al. (U.S. Patent No. 6,077,758) in view of Zhang et al. (U.S. Patent No. 5,529,937) and claims 25-26 are rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claim 1 of Zhang et al. (U.S. Patent No. 6,077,758) in view of Yamazaki (U.S. Patent No. 6,197,624B1). These double patenting rejections are respectfully traversed for the same reasons provided above in the responses to the §102(e) and the §103(a) rejections and regarding the deficiencies of Yamazaki et al.

New dependent claims 88-171 have been added to complete the scope of the invention to which Applicants are entitled.

CONCLUSION

Having responded to all rejections set forth in the outstanding Final Office Action, it is submitted that claims 15-26, 28, and 30-87 and new claims 88-171 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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VERSION OF AMENDED CLAIMS WITH
MARKINGS TO SHOW CHANGES MADE

15. (Amended) A method of fabricating a semiconductor device [including a thin film transistor, wherein the thin film transistor is formed through the steps of] comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film;

carrying out a second heat treatment for the crystalline semiconductor thin film at 900 to 1200°C in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film.

17. (Amended) A method of fabricating a semiconductor device [including a thin film transistor, wherein the thin film transistor is formed through the steps of] comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film; and

carrying out a second heat treatment for the crystalline semiconductor thin film in a reducing atmosphere including a halogen element to flatten a surface of the crystalline semiconductor thin film.

20. (Amended) A method of fabricating a semiconductor device [including a thin film transistor, wherein the thin film transistor is formed through the steps of] comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film;

carrying out a second heat treatment of irradiating the crystalline semiconductor thin film with ultraviolet light or infrared light; and

carrying out a third heat treatment for the crystalline semiconductor thin film at 900 to 1200°C in a reducing atmosphere to flatten a surface of the crystalline semiconductor thin film.

22. (Amended) A method of fabricating a semiconductor device [including a thin film transistor, wherein the thin film transistor is formed through the steps of] comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film;

carrying out a second heat treatment of irradiating the crystalline semiconductor thin film with ultraviolet light or infrared light; and

carrying out a third heat treatment for the crystalline semiconductor thin film in a reducing atmosphere including a halogen element to flatten a surface of the crystalline semiconductor thin film.

25. (Amended) A method of fabricating a semiconductor device [including a thin film transistor, wherein the thin film transistor is formed through the steps of] comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film;

selectively providing the crystalline semiconductor thin film with an element of group 15;

carrying out a second heat treatment to getter the catalytic element into a region of the crystalline semiconductor thin film selectively provided with the element of group 15;

patterning the crystalline semiconductor thin film into at least one crystalline semiconductor island to become at least a channel formation region by removing at least the region of the crystalline semiconductor thin film selectively provided with the element of group 15; and

carrying out a third heat treatment for the at least one crystalline semiconductor island at 900 to 1200°C in a reducing atmosphere to flatten a surface of the at least one crystalline semiconductor island.

28. (Amended) A method of fabricating a [crystalline] semiconductor [thin film, comprising the steps of] device comprising:

adding [a catalytic] an element for facilitating crystallization of an amorphous semiconductor thin film to at least a portion of the amorphous semiconductor thin film;

carrying out a first heat treatment to transform the at least a portion of the amorphous semiconductor thin film into a crystalline semiconductor thin film; and

carrying out a second heat treatment for the crystalline semiconductor thin film at 900 to 1200°C in an atmosphere containing hydrogen therein to flatten a surface of the crystalline semiconductor thin film.

30. (Amended) A method of fabricating a semiconductor device comprising:

forming a semiconductor film comprising silicon over a substrate;

crystallizing said semiconductor film;

[etching a surface of said semiconductor film after said crystallizing step to remove an oxide therefrom;]

subsequently heating said semiconductor film provided with an oxide formed on a surface thereof in [inactive] an atmosphere which reduces said oxide formed on said surface [after said etching step while exposing said semiconductor film to said inactive atmosphere].

31. (Amended) A method of fabricating a semiconductor device comprising:

forming a semiconductor film comprising silicon over a substrate;

crystallizing said semiconductor film;

[treating a surface of said semiconductor film with hydrofluoric acid after said crystallizing step to remove an oxide therefrom;]

subsequently heating said semiconductor film provided with an oxide formed on a surface thereof in [inactive] an atmosphere which reduces said oxide formed on said surface [after said treating step while exposing said semiconductor film to said inactive atmosphere],

wherein said atmosphere comprises hydrogen.

34. (Amended) A method of fabricating a semiconductor device comprising:

forming a semiconductor film comprising silicon over a substrate;

crystallizing said semiconductor film;

[etching a surface of said semiconductor film after said crystallizing step to remove an oxide therefrom;]

subsequently heating said semiconductor film provided with an oxide formed on a surface thereof at a temperature of 900 to 1200°C [after said etching step] in an atmosphere which reduces said oxide formed on said surface.

35. (Amended) A method of fabricating a semiconductor device comprising:

forming a semiconductor film comprising silicon over a substrate;

crystallizing said semiconductor film;

[treating a surface of said semiconductor film with hydrofluoric acid after said crystallizing step to remove an oxide therefrom;]

subsequently heating said semiconductor film provided with an oxide formed on a surface thereof at a temperature of 900 to 1200°C [after said treating step] in an atmosphere which reduces said oxide formed on said surface,

wherein said atmosphere comprises hydrogen.